A NEW, SPECIFICALLY MONOLITHIC APPROACH TO MICROWAVE POWER AMPLIFIERS

D. Pavlidis, Y. Archambault, M. Efthimerou,
D. Kaminsky, A. Bert, J. Magarshack

Thomson-C.S.F./D.C.M., Domaine de Corbeville, B.P. 10
91401 ORSAY, France

ABSTRACT

A new principle was used to build a GaAs MMIC, X-band Power Amplifier based on a modular tree design where the number of modules increase at each amplifying stage. First experimental data show 10 dB gain at the centre of the operating band (8 - 9 GHz).

INTRODUCTION

Monolithic power amplifier designs have been inspired by microstrip hybrid circuits (1) and by I.C. analog designs (2). High power levels require FET devices with very large peripheries in the last amplifying stages. The size of the device cannot, however, be indefinetely increased without consequences on the amplifier performance. Depending on the frequency of operation, the total gate periphery is limited to a maximum value which allows safe operation without phasing, crosstalk and oscillation problems. In an effort to minimise the above effects, designers have developed divider/combiner circuits (3) with more than 90 % efficiencies and reasonable isolation and phase equalisation characteristics. Other designs (4) use the "cell cluster matching" approach, where input matching is done at the level of every individual "cell cluster", which is then partially matched at the output before combining via $\lambda/4$ transformer lines.

The alternative approach presented here uses the "cell cluster" principle but instead of driving a large array of clusters, it utilises several amplifier stages consisting of a plurality of identical cells. Each cell has one input (gate) and two or more outputs (drains) feeding the input of the next stage cells. The matching circuits connecting each output to the corresponding input of the next stage are the same all over the amplifier. The input cell impedance remains at the same high level as long as the signal is divided and amplified. This amplifier topology is relatively insensitive to phasing and oscillation problems due to the FET cell inherent isolation characteristics and the relative equality of the signal levels at each module even for high gain amplifiers.

AMPLIFIER ANALYSIS

GENERAL ANALYSIS AND PREDICTED PERFORMANCE

The amplifier design was based on S-parameter data obtained by characterising discrete GaAs FETs from 2 to 18 GHz. Fig. 1 shows a simple FET equivalent circuit model derived by an in house developed optimisation programme which guarantees an average deviation of 2% between experimental and modeled S-parameter values. The circuit element values correspond to FET devices with 200 µm gate width and 1.5 µm gate length. These devices had two 100 µm wide gate fingers and two were paralleled to form an amplifier cell with 400 µm total gate periphery. A photograph of the device together with its geometry details is shown in Fig. 2.

Using the equivalent circuit model of 200 µm and 400 µm devices and optimising with COMPACT and ESOPE several three and two stage amplifiers were designed in the frequency band of 8 to 9 GHz. The new, specifically monolithic approach uses several separate FET cells at each amplifier stage, so that instead of increasing the dimension of a unique transistor as the power hierarchy increases by paralleling up more cells, each amplifier stage consists of a plurality of identical cells each one having a single input (gate) and two outputs (drains) ; each output feeds another similar cell with a single input and two outputs and so on. In other words, instead of the power level per unit area increasing at each stage, the power level per cell remains more or less constant but the number of cells increases.

The design goal for the three stage amplifier was a flat 20 dB gain from 8 to 9 GHz. The optimized circuit topology is shown in Fig. 3. The input and output matching networks include a capacitor which insures d.c. decoupling, a transmission line and a lumped inductor. Similar matching topologies were used for the interstage network ; the impedance to be transformed here is the input impedance of the output or interstage FET. Gate biasing of the interstage and output FETs is accomplished by integrated 2 KΩ bias resistors which reduce the overal gain by only 0.5 dB. The design is accomplished by maximising the gain and matching the input and output across the 8 to 9 GHz band.

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Fig. 4 shows the calculated gain-frequency response of the three stage amplifier together with its input and output VSWP. The predicted gain is 25.8 dB at the operating band centre but reduces to about 16.6 dB by considering the low quality factor ($\sim$ 20) of the lumped matching/bias inductors.

The relatively high inductance values imposed by the optimisation could only be realised by lumped elements. Computer routines were developed in order to evaluate the necessary inductor geometries taking into account the earth parasitics which are very important for monolithic desings on 100 µm thick GaAs substrates. Capacitors were of the overlay type and their geometries were estimated on the basis of low and high frequency Si_3N_4 measured data. These elements were also used to provide d.c. decoupling between stages. Bias resistors for the gates were made in integrated from and their geometry was determined by sheet resistance data, $\sim$ 800 Ω/□ for the GaAs layers used.

AMPLIFIER LAY - OUT

A photograph of a completed amplifier chip is shown in Fig. 5. Amplifier dimensions are 2.8 mm X 2.6 mm. The circuit posesses a central symmetry with respect to its X - axis. FET sourcesof each circuit half are interconnected with dielectric bridges and extended up to the chip edges. RF bypass for the tuning loop inductors is provided by earth connected integrated overlay capacitors with nominal values exceeding 2 pF.

Gate bias voltage is provided from a common terminal point by 10 µm wide microstrip lines which cross over certain RF paths of the amplifier. The parasitic capacitance introduced by such crossovers is estimated to be of the order of 0.12 pF. The bias lines are connected through 2 kΩ resistors to the FET gates at the input tuning capacitor points. Cell isolation of the last output stage is improved by the inclusion of theses resistors wich minimise cell interactions and assure performance stability.

PERFORMANCE CONSIDERATIONS AND PARAMETER SENSITIVITY

To study the performance characteristics of the presented monolithic amplifier approach, FET cells with the split drain output configuration, as employed in the design, were individually characterised over a large frequency band (2 to 18 GHz). It was found that the S_{21} and G_{max} of the one half of the cell (drain D1) was not influenced by impedance variations at the drain D2 of the other half, event when extreme terminating conditions such as 50 Ω to 0Ω were used. Some influence on the S_{21} and G_{max} characteristics of the cell D1 was observed when biasing the other half cell D2 between 0V and V_d but this was on the average less than 1 dB all over the frequency band : this effect can be explained by backgating considerations which are confirmed by observing a change in the operation point of the cell D1 when cell D2 is biased on and off. Isolation between drains varies between 21 dB and 32 dB over the frequency band , and is more frequency dispersive in the case of bad input gate matching conditions deteriorating, however, in all cases not more than 18 dB.

The above tests show that any parameter variation between FET cells will have negligible influence on neighbouring devices. Neither circulating currents and thus losses, nor reflection interractions by improperly matched individual cells can therefore have any influence on the amplifier performance. The performance degradation due to FET failure, has been simulated with the help of ESOPE. The results show that failure of any intermediate FEL cell causes a gain drop varying between 0.5 dB (opened gate) and 1.2dB (shorted gate), and has negligible influence on the input and output VSWR. The amplifier is immune to failure of any one of the output cells, while its performance is catastrophically degraded in case of input FET failure.

The problem of matching low impedance devices such as large arrays of paralleled FETs, especially at the output stages of conventional amplifiers is overcome by the inherent property of the presented amplifier principle where similar modest width and thus reasonable input impedance devices are used for all stages. The same argument is valid for the phasing problems which are likely to occur in large FET chips.

The performance degradation by circuit element deviations from the considered nominal values has also been simulated, assuming ± 10% variations. The largest influence seems to come from improperly designed inductors. The centre frequency of the 8 to 9 GHz three stage amplifier changed by $\Delta f = \pm$ 450 MHz, the average gain over the operating band was reduced by up to ΔG = 2 dB and the gain flatness was deteriorated when inductor values were assumed to vary between ± 10% of their nominal values.

When capacitor values were allowed to vary between ± 10% of their nominal values, the centre frequency changed by $\Delta f = \pm$ 300 MHz, the average gain was reduced by up to 1.5 dB and the amplifier flatness was less drastically deteriorated.

The simultaneous variation of the C's and L's by + 10% in the opposite way tends to produce ΔF = + 400 MHz, ΔG = 2 dB and serious gain flatness deterioration as in the single inductor variation case. If both C and L values vary in the same way i.e both + 10% or both -10% of the nominal value then Δf = + 500 MHz, ΔG = 2 dB and again serious flatness deterioration is observed.

AMPLIFIER FABRICATION

The amplifier fabrication process is based on the MMIC technology features currently used by many laboratories. MMIC fabrication starts by device isolation on either commercially available VPE grown active layers or ion implanted in house grown LEC GaAs substrates. Isolation is achieved by boron implantation at 60 keV and 130 keV energy levels with a 1 X 10^{13} cm^{-2} and 2 X 10^{13} cm^{-2} doses respectively.

AuGe/Pt ohmic contacts are then defined by lift-off for the source and drain of the FET cells, the two contacts being separated by 4.5 µm in the channel region. Following the annealing of the ohmic contacts at 470°C, the device gates are defined and a 500 Å Ti/ 1000 Å Pt/ 3000 Å Au /500 Å Ti layer is evaporated to form 1.3 µm long gates by lift - off. The same metallisation is also used to cover the source and drain contacts and improve their conductivity. At the same time several other parts of the circuit are defined such as capacitor bottom plates and bridge interconnections. The thin Ti layer included in the Schottky metallisation improves the adhesion of the 4000 Å thick silicon - nitride sputtered layer which is deposited in the following step all over the wafer. This Si_3N_4 layers form the capacitor dielectric, as well as, the isolation layer for the bridge crossovers. It is also used to protect the active layer of the FET devices.

Following dielectric deposition, a new photolithography step defines the areas where interconnections will occur between first level Schottky metallisation and the following second level. The areas where the dielectric is conserved are covered by photoresist and the exposed dielectric is removed by plasma etching in an CF_4 atmosphere.

Capacitor top plates, inductor elements, transmission lines and source interconnections are all simultaneously deposited by lift-off in the following level, where a layer of 1000 Å Ti/ 1000 Å Pt/ 2.0 µm Au is evaporated into the openings of a double photoresist structure separated by a thin Ti layer ; this structure gives good overhang for lift-off of the 2.0 µm thick Au layer.

The wafers are finally thinned to 100 µm, metallised with Ti/Au on the back and cut to individual amplifier chips. Mounting is done on specially developed microwave packages with the aid of Ag/Sn solder.

Test patterns are fabricated together with the amplifier chips and allow the complete characterisation of the processing steps (ohmic contact, sheet resistance of active layer and metallisations, electric testing of misalignment, mobility calculation and FET model parameter estimation). In addition to these patterns, the FET cells are repeated in discrete form together with an array of Si_3N_4 capacitors in order to perform static tests.

AMPLIFIER EXPERIMENTAL PERFORMANCE

The wafers were characterised with the aid of the test patterns and a first selection of amplifier chips was made on the basis of these data and visual inspection. The amplifiers finally chosen for microwave characterisation were also tested for correct drain voltage distribution over the circuit, as well as, proper gate control.

The chips were mounted in a brass carrier which was inserted between two 100 µm thick alumina substrates of a test fixture. The dc bias networks were all included in the amplifier and therefore only two bonds were required for biasing : gate and drain bias bond. The chipscontain in integrated form :seven FETs, 17 dielectric capacitors, 11 dielectric bridges, 6 active bias resistors, and 8 loop inductors.

The final version of the amplifier seen in Fig. 5 includes mask modifications of the final metallisation level which were necesseray to make the amplifier operate at the desired frequency band. The main reason for the frequency discrepancies were incorrect prediction of passive element values ; the first geometries were selected on the basis of purely theoretical data but precise microwave characterisation of a large number of passive components enabled the correct choice the second time.

First experimental data show a gain and frequency response as in Fig. 6. The amplifier has a gain of about 10 dB at midband and a V.S.W.R. of the order of 3 : these data give the overall performance of an as mounted amplifier. Later results will be presented.

CONCLUSIONS

The design, fabrication and performance of a 8 - 9 GHz three stage monolithic GaAs FET amplifier based on a modular tree principle is demonstrated. The amplifier has an integral bias network and only two RF bonds and two dc-bias bonds. First results show a 10 dB gain at midband. The dimensions of the chips are 2,6 mm X 2,8 mm X 0,1 mm. This amplifier demonstrated the ease of implementing the design and shown the feasibility of the new principle.

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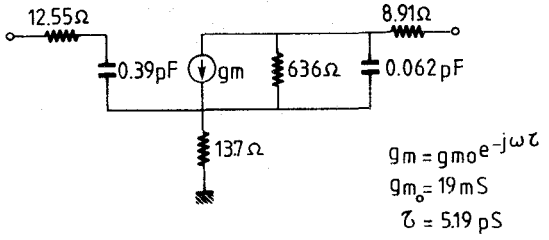

Fig 1: Equident circuit model of 200µm wide FET

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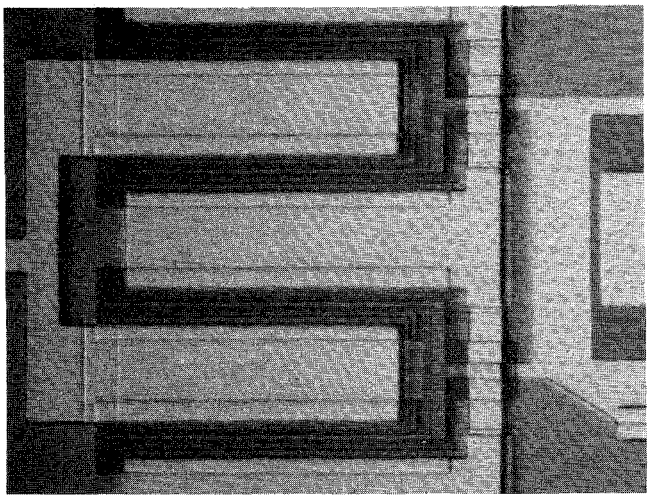

Fig 2: Photograph of 400µm FET cell (×500)

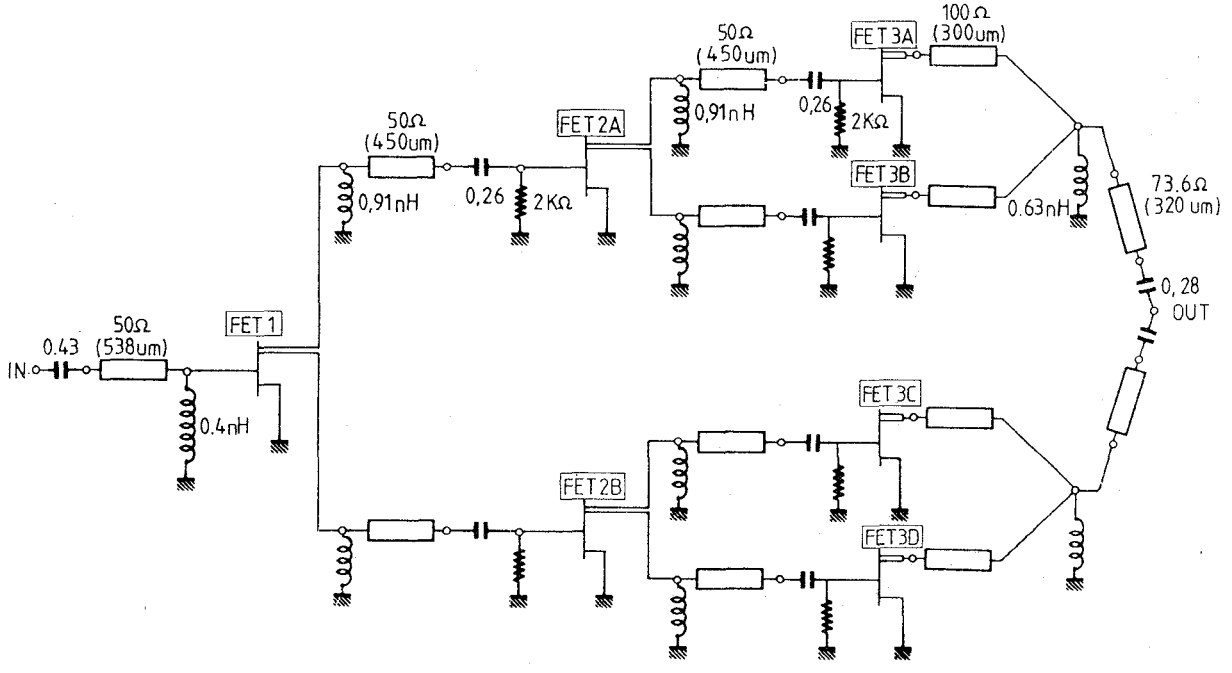

Fig 3: Amplifier circuit topology

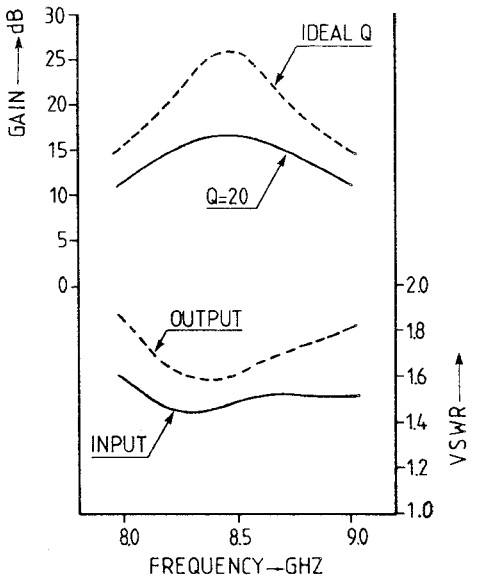

Fig 4: Gain, Input and Output VSWR frequency response of the 3-stage amplifier

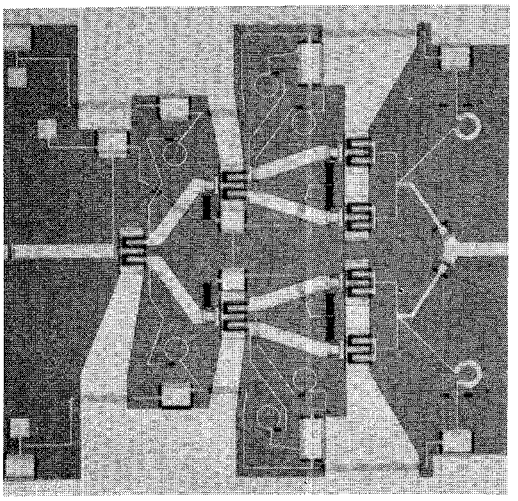

Fig 5: Photograph of the 3-stage amplifier (Chip size 2,6 mm × 2,8 mm)

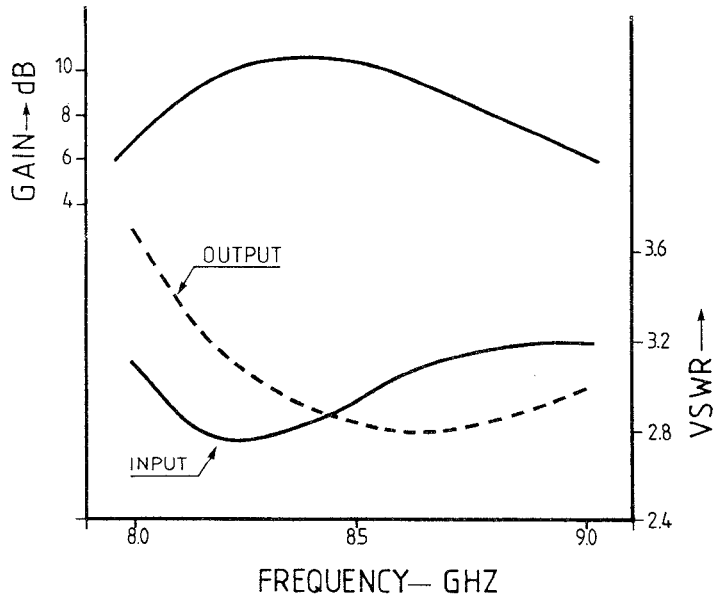

Fig 6: First overall performance of the 3-stage amplifier